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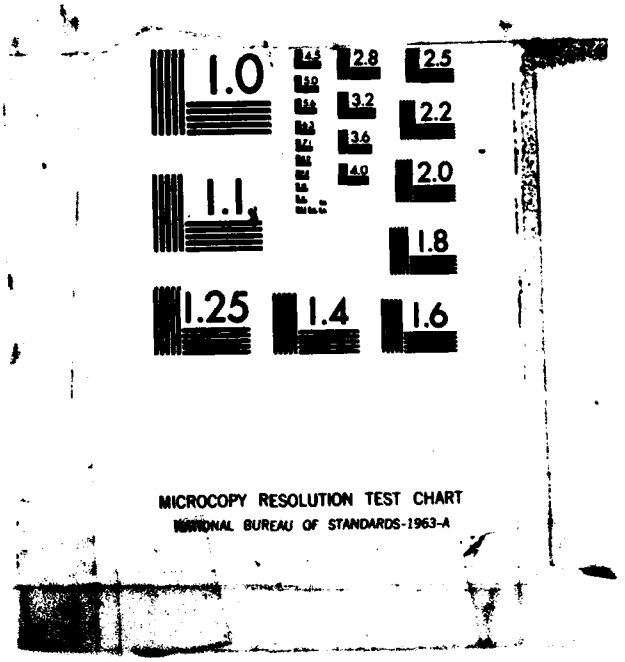
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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER: ~~AFOSR-TR-~~ 83-1215
2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER

4. TITLE (and Subtitle): Development of Short Gate Fet's
5. TYPE OF REPORT & PERIOD COVERED: Annual June 82-June 83
6. PERFORMING ORG. REPORT NUMBER

7. AUTHOR(s): Dr. Michael G. Spencer
8. CONTRACT OR GRANT NUMBER(s): AFOSR-81-0223

PERFORMING ORGANIZATION NAME AND ADDRESS: Dept of Electrical Engineering, School of Engineering, Howard University, 2300 Sixth St. N.W. Washington D.C. 20059
10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 61102F, 2305/C1

CONTROLLING OFFICE NAME AND ADDRESS: Air Force Office of Scientific Research, Air Force Systems Command, USAF /NE, Bolling AFB DC 20332
12. REPORT DATE: DEC 83
13. NUMBER OF PAGES: 19

MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)
15. SECURITY CLASS. (of this report): Unclassified
15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

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17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Annual results on research for development of short gate FET's is reported. High material purity was obtained on in house liquid phase and vapor phase reactors. Quarter micron metal lines have been fabricated using deep uv lithography.

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AFOSR-TR- 83-1215

DEVELOPMENT OF SHORT GATE FET'S

ANNUAL REPORT
December 1983

Howard University
Washington, D.C. 20059

RESEARCH OBJECTIVES

The principal objective of this research is to try to understand the performance limitations of a standard planar GaAs field effect transistor. The primary interest in this work is to experimentally try to see to what extent hot electron phenomena enhances the device performance. In addressing these primary issues auxillary research objectives have manifested. One auxillary objective is to see if deep uv lithography can be used as a viable processing technology in the .25um region. Another related objective is to understand the nature of the GaAs material defects and their effect on device performance.

PROGRESS

In this section we will describe the progress, to this point, in meeting the above-mentioned research objectives. This will be divided into three major areas: materials development, deep uv lithography development and materials characterization studies. Finally, we will present our progress on a novel device structure which we have been pursuing for millimeter wave mixer diodes but has meaning for this work.

We have developed our LPE (liquid epitaxy system) technology during this period of the contract. Now we can routinuely grow undoped epitaxial layers with liquid nitrogen mobility in excess of 120,000 cm^2/v-sec. These layers have been characterized by hall mobility (see Table 1) measurement as well as by photo-luminescence and DLTS. These layers show well defined excition structure and no electron traps. Standard one and two micron fet's with undoped buffer layers have been fabricated using this system. In addition, this material is being used as a base material for materials studies which will be expanded later. This system is also available for future hybird of material growths. In addition to liquid phase growth, we are now in the process of optimizing the growth parameters of our $AsCL_3$ vapor epitaxial system. Finally, construction on our MOCVD reactor continues and we anticipate the first epitaxial layers from this system in approximately four months. Initially we intend to use the LPE and Vapor Phase System to provide active layers to experiment with device concepts. Later the active layer will be grown by MOCVD or MBE.

We have been developing our deep uv lithography processing. A fet mask set as well as a test pattern mask set has been produced by electron beam lithography and wet chemical etching. Both mask sets have feature sizes as small as .25um. Initially we sought to determine our processing parameter. Figure 1 shows the development of PMMA in MIKB as a function of exposure time and development time. From these experiments we were able to approximate our optimum parameters. We then went on to adapt a copolymer technique which was orginally used with E-beam lithography. This technique produces a resist profile suitable for lift-off. Figures 2 & 3 show patterns in metal that were produced by this technique. Calibration masks on the microscope show the dimensions to be on the order of .25 micron. Appendix I contains a report submitted to the National Submicron Center summarizing our deep uv results.

We have been conducting two interactive projects with the Naval Research Laboratories in the area of materials characterization which have some meaning for this work. First, we have been providing LPE material as a base for doing neutron irradiation studies. Since LPE material has no electron traps as grown it provides a good medium for assesing the introduction of deep levels into GaAs. In this study LPE material is grown and characterized by CV, Hall and DLTS techniques. The material was irradiated with various neutron fluences. The resulting material is now being characterized as irradiated after various low temperature annealing cycles. These experiments are yielding information on the neutron defect introduction rate and shedding some new light on the possible connection of the "EL2" level and the GaAs antisite defect. A second experiment now beginning in conjunction with the Naval Research Laboratory concerns the characterization of O_2 implanted material using luminesence. The value of the LPE material is that it isolates the defect luminescence of the substrate from the luminescence possibly due to substitional O_2.

We are pursuing the fabrication of GaAs mixer diodes by a technique in which etched troughs are filled in by LPE. We are being aided in this effort by MBE layers (used for the active region) grown at Naval Research Laboratories. We intend to pursue similar types of structures for this work. (This work was submitted to WOCSEMMAD. See appendix II for abstract).

Finally we are beginning initial fabrication of submicron structures. These structures will be "simple" fet structures with no n^+ layers. They will have gate dimensions of 1/2 and 1/4 micron. After these initial structures we intend to pursue some novel ways of putting in the n^+ regions.

In summary we have developed the materials and lithography capability to fabricate submicron fet's. Construction of the devices is proceeding. In addition, we are conducting several collaborative experiments to better understand GaAs material and material processing.

TABLE I

Sample Number	Thickness (um)	Mobility ($cm^2v^{-1}s^{-1}$) 300°K	Mobility ($cm^2v^{-1}s^{-1}$) 77°K	Carrier Concentration (cm^{-3}) Net
HU2	4	4,000	33,000	2×10^{14}
HU5	8	5,000	65,500	4×10^{14}
HU4	15	7,500	80,000	3×10^{14}
HU8	10	7,800	101,000	2×10^{14}
HU9	15	8,000	110,000	3×10^{14}
HU7	9	11,000	120,000	8×10^{13}

Hall data on undoped n-type GaAs films grown at various temperatures.

APPENDIX I

DEVELOPMENT OF SHORT GATE FET DEVICES

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The aims of this research are to determine the limits of performance of a standard GaAs field effect transistor and to ascertain whether these structures (made with submicron dimensions) could be produced effectively by deep uv lithography. This technical abstract will concentrate on the latter objective.

A test pattern mask set and a transistor mask set were produced at the National Submicron Center by using e-beam lithography followed by wet chemical etching. The Cr covered quartz plates were supplied (with pmma) by the Hoya Co. The thickness of the Cr was approximatly 800 angstroms. We also attempted to fabricate masks using evaporated Cr. Excellent results were obtained using the Hoya plates. Line widths as small as .22 microns were defined. Equivalent results could not be obtained using the evaporated Cr.

Several exposures were done using the test pattern mask described above. The substrates were coated with 2500 angstroms of 4% pmma and were developed in a 1:1 solution of mibk and propanol. Figure 1 shows the results obtained as a function of exposure time and development time. Optimum parameters were exposure times of approximately 3.5 minutes for development times of about 2 minutes.

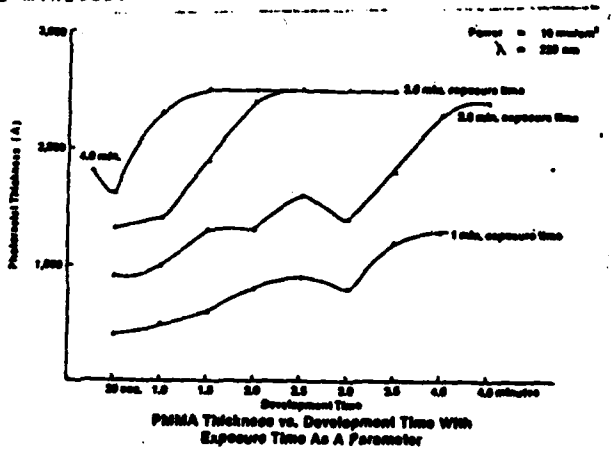

Figure 1. Development of 2500 angstroms of 4% pmma in mibk and propanol as a function of exposure time and development time.

A co-polymer technique developed for e-beam lithography was adapted for deep uv lithography[1,2]. The top layer of resist was 2500 angstroms of pmma while the lifting layer was 5000 angstroms of pmma-pmaa. The advantage of this double resist technique lies in the ablity to develope the layers seperately. This allows for the production of a resist profile suitable for lift off. Optimum exposure times appear to be in the range of 4 to 5 minutes (for our bulb intensity). Figure 2 shows a .25 micron metal FET gate which was produced using the co-polymer technique.

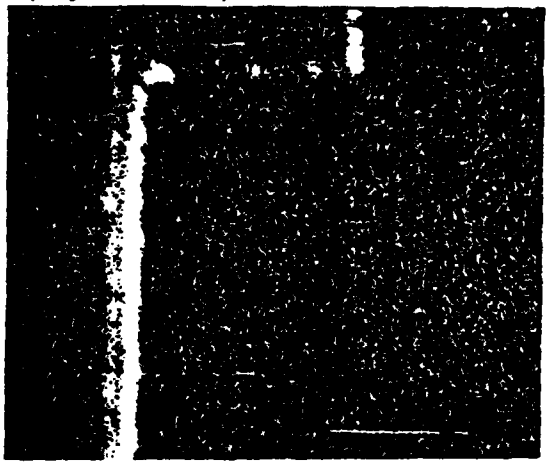

Figure 2. Metal gate of submicron field effect transistor. The calibration mark on the electron microscope indicates a length of one micron.

In summary we have produced high resolution e-beam masks suitable for deep uv lithography. We have used these masks for system calibration as well as to define submicron geometries in metal.

1.) M. Hatzakis U.S. Patent 4,024,293 (1977)
2.) M. Hatzakis J. Vac Sci Technology Vol 16 p. 1984(1979)

APPENDIX II

TWO NOVEL GROWTH AND FABRICATION TECHNIQUES FOR MILLIMETER-WAVE MIXER DIODES

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Abstract - Two novel techniques have been developed to fabricate surface-oriented millimeter-wave GaAs mixer diodes. These techniques eliminate and/or reduce many of the problems associated with other fabrication techniques(1) such as proton bombardment, selective epitaxy, and etched mesa formations. The techniques produce "pockets" of conducting epitaxial material within regions of non-conducting material, while maintaining a quasi-planar surface for device fabrication. The first technique produces n/n+ conducting pockets in semi-insulating GaAs by chemically back-etching an MBE layer grown on the substrate surface, while preserving the same MBE layer grown into previously etched pockets (Figure 1). The second technique produces n/n^+ conducting pockets by chemo-mechanically polishing away an LPE layer grown on the substrate surface, while preserving the same LPE layer grown into previously etched pockets (Figure 2).

The quality of the layers grown into the pockets of both techniques were found to be morphologically and electrically good. It was discovered that discontinous growths did occur near the hole edges for thick layers using the first technique, however no discontinuous growths were discovered using the second technique for layers grown as thick as 12um. As a result of this phenomenon, the conducting and non-conducting surface regions obtained using the second technique were found to be of exceptionally high definition and planarity.

Mo/Au Schottky-barrier diodes with 2um-diameters fabricated onto these epitaxial layers ($n \cong 3x10^{16} cm^{-3}$ and $n^+ \cong 3x10^{18} cm^{-3}$) have produced good preliminary results. DC measurements taken on devices of the first technique have yielded a maximum zero-biased cutoff frequency (F_{CO}) of 2200 GHz with a series resistance (R_S) of 6Ω and a zero-biased capacitance (Co) of 13fF. DC measurements taken on devices of the second technique have yielded F_{CO} of 700GHz for values of R_S and C_O as low as 9Ω and 25fF respectively.

1. B.J. Clifton, "Monolithic integrated receiver technology for the millimeter and submillimeter wave regions", Proc. of Eighth Biennial Cornell Eng. Conf. (Ithaca,N.Y.), vol.8, pp. 1-12, August 1981.

This work is supported in part by the National Aeronautical and Space Administration and the Office of Naval Research.

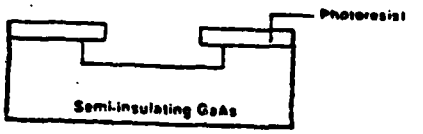


Figure IA. Chemically etch pocket.

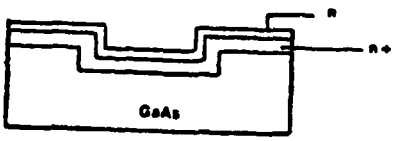


Figure IB. Epitaxial layer growth into pocket.

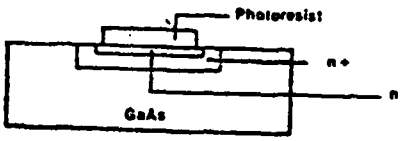


Figure IC. Removal of excess epitaxial material.

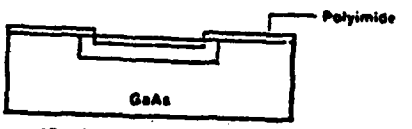


Figure ID. Deposition of oxide layer.

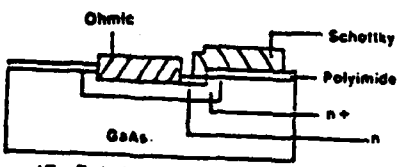
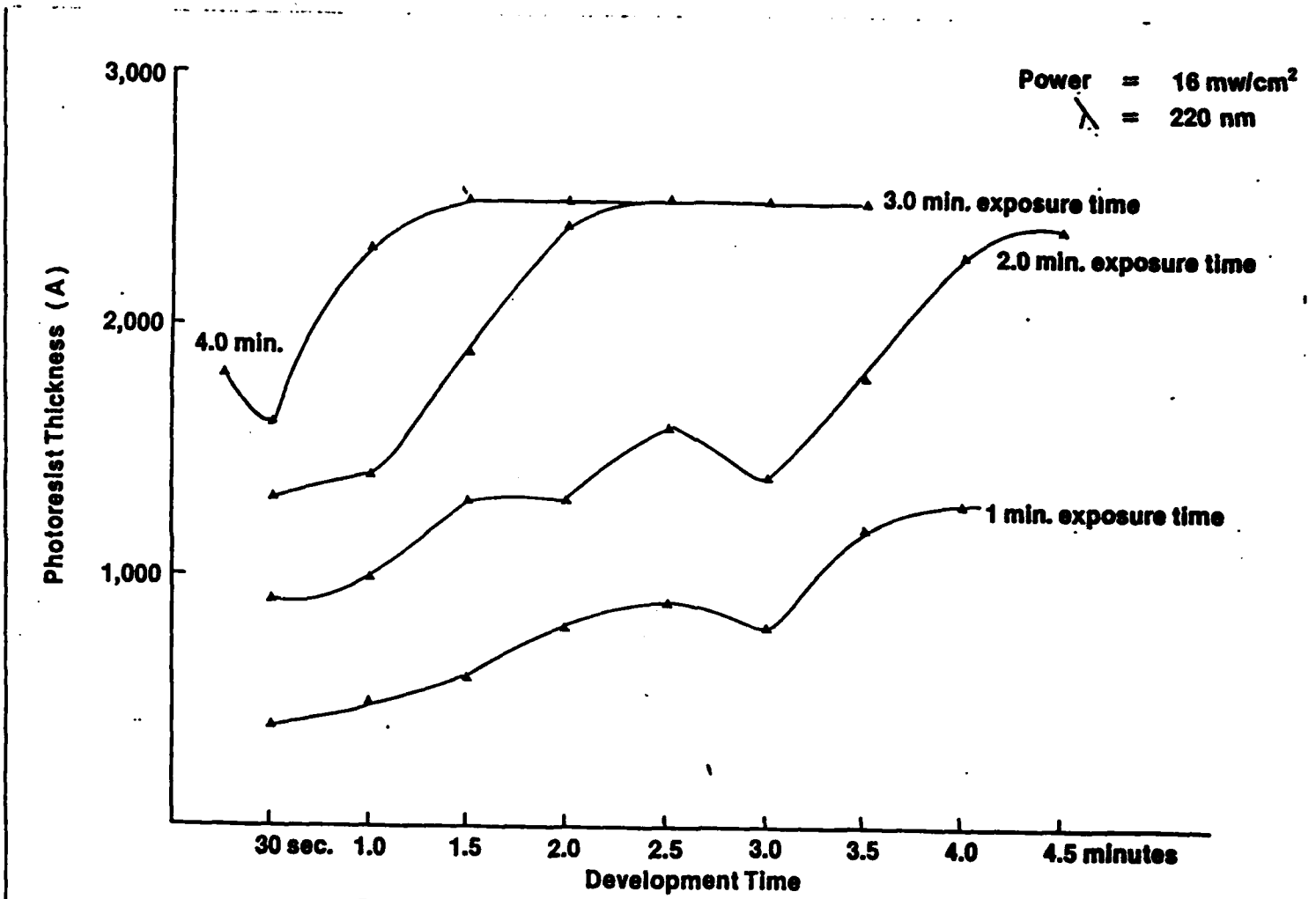


Figure IE. Fabrication of ohmic and schottky contacts.



PMMA Thickness vs. Development Time With Exposure Time As A Parameter

Figure 1

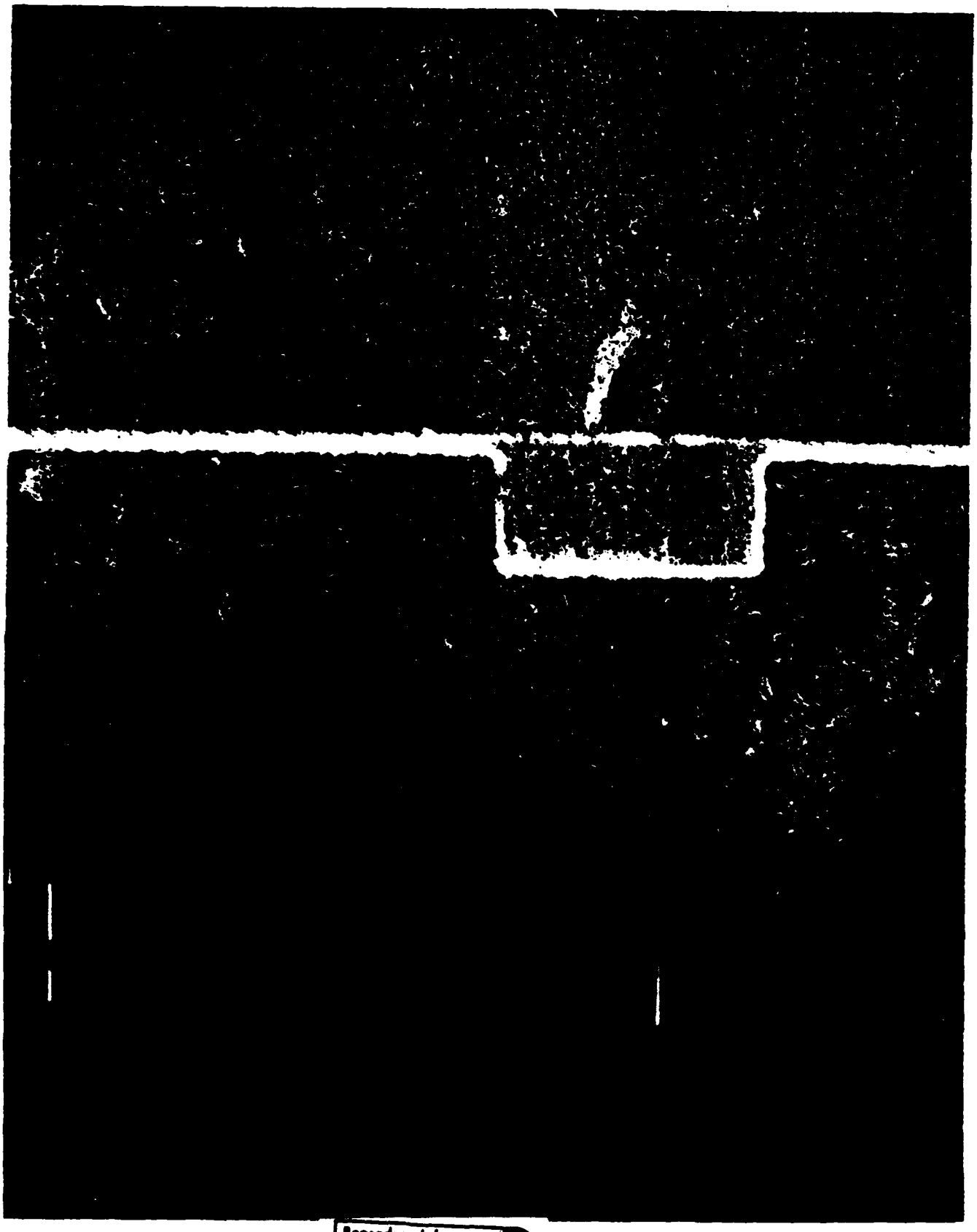


FIGURE 2

Metalized submicron gate structure calibration mark (longer line) is one micron.

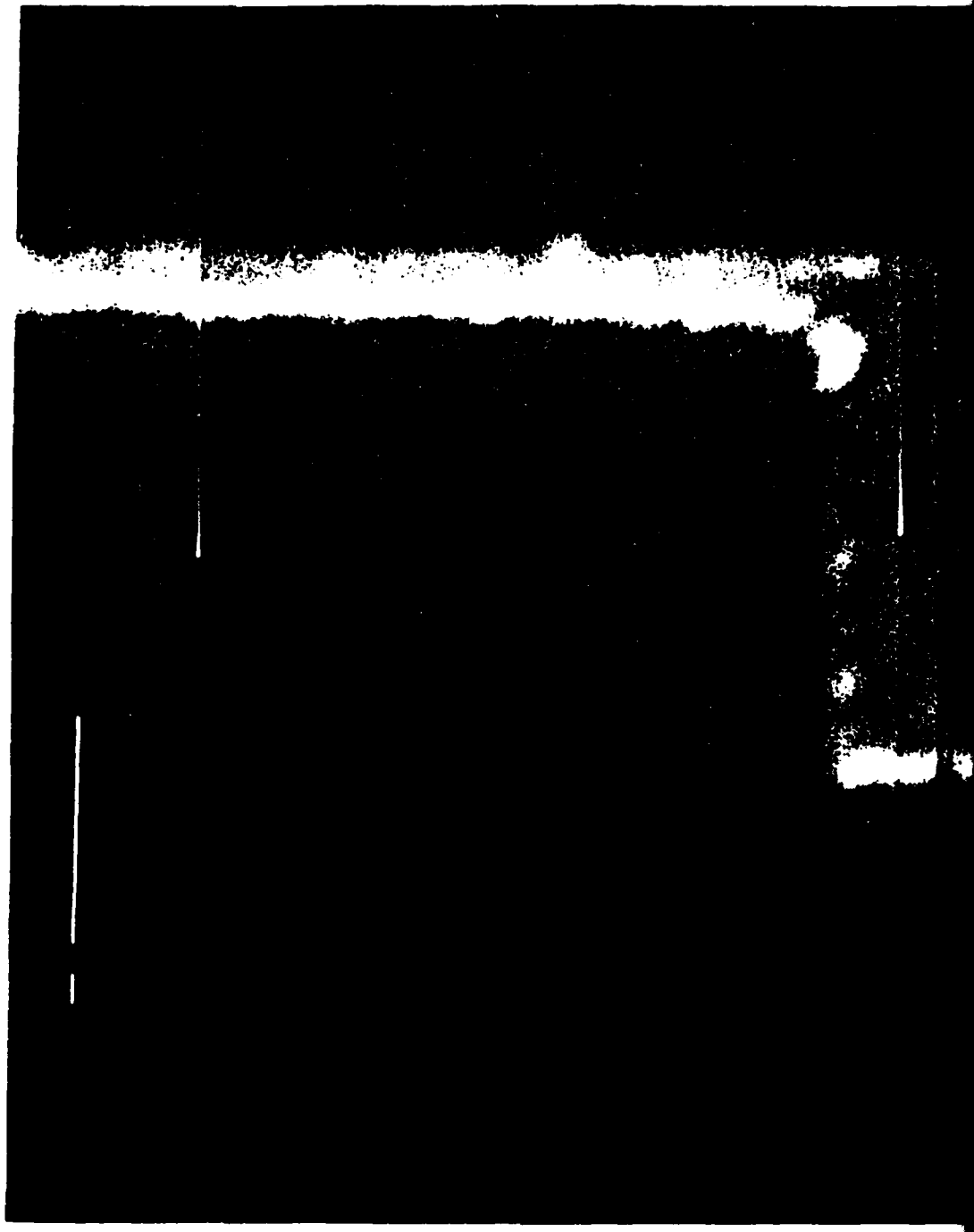


FIGURE 3

Metalized submicron gate structure calibration mark (longer line) is one micron.

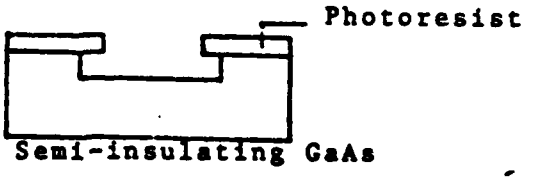


Figure 2A. Chemically etch pocket.

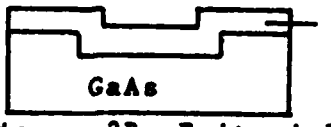


Figure 2B. Epitaxial layer growth into pocket.

Figure 2C. Removal of surface n^+ by polishing.

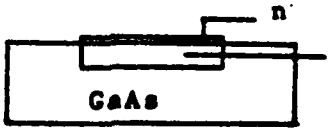


Figure 2D. Growth of ultrathin n-layer.

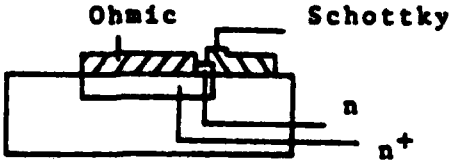


Figure 2E. Fabrication of ohmic and Schottky contacts.